

ANNEXE 4

English version of the document:

CCTP_A06_Annexe-1_ Tests HALT&HASS_KM3NeT_FR Version

SUBJECT:

This document describes the HALT and HASS tests designed to ensure high reliability of KM3NeT products.

Lot n°06

CLB-V6 Electronic Cards

CONTENTS

Definitions.....	3
1 Introduction.....	4
1.1 Highly Accelerated Life Test.....	4
Testing Beyond the Failure Point	6
Recording Failures.....	6
1.2 Highly Accelerated Stress Screening	6
2 Documentation used	7
3 Highly Accelerated Life Tests For KM3NeT.....	7
3.1 Requirements	7
3.2 Description and procedure of the HALT test.....	8
3.2.1 Minimum tests.....	9
3.2.1 Optional tests	10
3.3 HALT DOCUMENTATION	10
4 HASS.....	11
4.1 Requirements	11
4.2 Description and procedure of the HASS test	11
4.2.1 Temperature (and vibration).....	11

Definitions

DL : Destruct Limit. = Limite de destruction.

It is defined as the level at which the product ceases to function and remains unusable under normal conditions of use.

OL : Operational Limit. = Limite opérationnelle.

It is defined as the last operational temperature or vibration set point before failure.

UOL : Upper Operation Limit = Limite supérieure de fonctionnement

UDL : Upper Destructive Limit = Limite destructive supérieure

LOL : Lower Operation Limit = Limite inférieure de fonctionnement

LDL : Lower Destructive Limit = Limite destructive inférieure

HALT : Highly Accelerated Life Test = Essai de vieillissement accéléré

HASS : Highly Accelerated Stress Screening = Criblage hautement accéléré des contraintes

ESS : Environmental Stress Screening = Dépistage du stress environnemental

1 Introduction

1.1 Highly Accelerated Life Test

Highly Accelerated Life Test (HALT) is a design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits. The main idea is to find weak points in the design in an early stage in order to correct them and improve and optimize the design in a reliable way.

This applies only to a few boards in the design stage. Ideally to a set of 4 to 6 boards

The goal would be to apply the HALT tests to the lower level of subassembly. At the top level of the assembly, the full object will be subject to qualification stress tests in a sequential way – possibly under monitoring according to the situation (as described below in this document). These qualification tests will be performed on a single unit.

Usually HALT tests can be implemented using several kinds of stresses such as thermal extremes, extreme thermal rates of change, vibration and the combination of thermal and vibration. Moreover, it could be used for other types of stress such as frequency margin, power supply loading, voltage margin or power cycling.

In the case of KM3NeT we will use thermal extremes, extremes thermal rates, and power cycling as minimum tests. Vibration, combined vibration plus extreme temperature rates of change are left as an option, recommended when possible.

During testing, it is essential to exercise product operation and ensure functionality. Test setups should be optimized to maximize functional test coverage.

The test setup should also allow for remote operation of the test and product from outside of the environmental chamber.

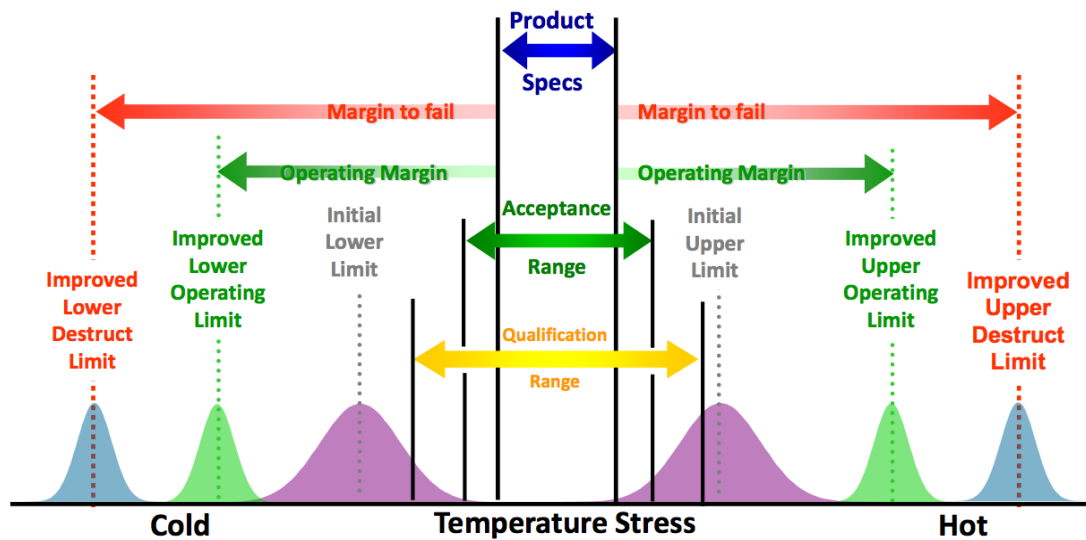


Figure 1: Graphical representation of the HALT / HASS different limits.

The ordering in which stresses are applied is governed by their likelihood of precipitating catastrophic failures. The following order is recommended.

1. **Thermal Extremes Stress:** Starting at the ambient temperature
2. **Thermal Extremes Stress:** Decreasing temperature at slow pace (5 degrees per step, at a rate lower than $1^{\circ}/\text{min}$) until the limits of the chamber (Phase I applied to CLB+PB). Allow stabilization of the temperature for 10 minutes at each step.
3. **Thermal Extremes Stress:** Increasing temperature at slow pace (5 degrees per step, at a rate lower than $1^{\circ}/\text{min}$) until the limits of the chamber (Phase I applied to CLB+PB). Allow stabilization of the temperature for 10 minutes at each step.
4. **Extremes Thermal Rates:** From initial temperature (ambient temperature) ramp quickly the minimum functional temperature detected in point 2 - or to the lowest temperature possible of the chamber-. The rates higher than $1^{\circ} / \text{min}$.
5. **Extremes Thermal Rates:** From initial temperature (ambient temperature) ramp quickly to the maximum functional temperature detected in point 3 - or to the highest temperature possible of the chamber-. The rates higher than $1^{\circ} / \text{min}$.

Optional tests:

6. **Vibration Stress:** Perform vibration tests.
7. **Vibration + Temperature Stress.**

Add **power cycling stress** in the previous tests (at each step).

Allow stabilization of the temperature for 10 minutes at each step.

Functional test at each step, before and after power cycling.

Minimum Sample Size - Multiple samples (**from 4 to 6 units**)

Testing Beyond the Failure Point

The HALT test should not stop when a failure is encountered. If possible, the failure mode should be analyzed and fixed to allow the test to continue beyond the stress level at which the failure occurred.

If a fix is not possible then testing should allow for and accommodate the known failure mode during further testing.

Note that the limits found during the HALT test will be used as reference for the HASS tests. **Therefore it is necessary to perform a HALT tests in a product in order to correctly define the HASS tests.**

Recording Failures

For each failure identified during testing, the following information should be recorded

- Failure point
- Failure description
- Root cause of failure mode
- Type of failure (catastrophic or recoverable)
- Class of failure (generic or non-generic)

1.2 Highly Accelerated Stress Screening

HASS tests are introduced to catch in a quick way those failures added during production that are not related to a faulty design.

The limits of temperature (and vibration if chosen) are set taking into account the HALT tests and the normal operating limits. The goal is to apply partial or limited stress to the product in order to avoid early failure.

Usually the limits are reviewed during the life of the devices to ensure that there is not under or over stress.

This is applied to 100% of the manufactured units at the beginning of the production but as production goes on it is possible to reduce to a part or batch of the components.

During HASS tests temperature stress is applied. If vibration is chosen then it is applied combined with temperature (temperature + vibration). Typically, the product is subjected to temperature ramping between its limits, with short dwells at extremes.

2 Documentation used

- IPC-9592 Performance Parameters for Power Conversion Devices
- MIL-HDBK-2164A - Environmental stress screening process for electronic equipment
- MIL-HDBK-338B - Electronic reliability design handbook

Bibliography

- *Doertenbach, Highly Accelerated Life Testing – Testing With a Different Purpose*
http://www.chromaate.com/chroma/webdrive/certificate/HLT_HASS/5_HighlyAcceleratedLifeTesting%E2%80%93TestingWithDifferentPurpose.pdf
- *Silverman, 10 Mistakes when performing HALT*
http://www.opsalacarte.com/pdfs/Tech_Papers/10_Mistakes_When_Performing_HALT_and_HALT_Integration.pdf

3 Highly Accelerated Life Tests For KM3NeT

3.1 Requirements

Highly Accelerated Life Testing (HALT) is performed as part of the **design process**.

In general, HALT stresses will be increased until the Target stress or a Physical limit is reached. Typically the stress applied to the product is **far beyond** what the product will encounter in a typical use environmental.

The HALT test will be applied to at least to a set of 4 to 6 boards, therefore differentiating with respect the HASS tests, that should be applied to all the products (at least at the early life of the product).

The following list shows which products should pass the HALT tests (*boards which design is intended to be improved*)

DOM Electronics

1. CLB (3.4.3.2)
2. PB (3.4.3.5)
3. Octopus (3.4.3.1.1 and 3.4.3.1.2)
4. PMT Base (3.4.2.2)

Power Electronics

5. BPS
6. DUL
7. VEOC DC /DC converter ARCA: PS_12V
8. VEOC DC /DC converter ORCA : Nikhef converter
9. OM
10. ORCA AC/DC converters

Base Module Electronics

11. CLB base (idem DOM)
12. FMC
13. RS 232 TTL converter?
14. Hydrophone
15. SCB board (WRS switching core board)
16. GBP (WRS carrier board for KM3NeT)

3.2 Description and procedure of the HALT test

The procedure to apply to the HALT tests of the electronics boards of KM3NeT will use temperature (minimum) and vibration (optional).

The following sets of tests will be applied:

Minimum tests:

- Temperature Step Stress
- Extreme Temperature Stress

Optional tests:

- Vibration Stress
- Temperature plus Vibration Stress

3.2.1 Minimum tests

Temperature Step Stress Tests

The procedure is defined with the following steps:

1. The device(s) is inserted in the climatic chamber and it is powered on.
2. The power consumption is measured
3. The correct behavior of the device is checked. (Functional tests are performed)
4. Starting at ambient temperature (ie 25 degrees), decreases of 5°C per step are applied. (1 degrees per minute -slow pace-).
5. Let the temperature stabilize for 10 minutes.
6. After each step, the behavior of the board is checked. (functional tests)
7. Before going to the next step (decrease of temperature) the board is switched off/on.
8. The behavior of the board is checked again (functional tests)
9. Continue decreasing temperature until failure of the lower temperature achievable by the climatic chamber is reached.
10. If possible to fix failure and continue decreasing temperature (except if the lower limit of the climatic chamber has been obtained)

4bis.- Starting at 25°C increase 5°C per step, 10 minutes, continue with the following steps but increasing temperature.

Extreme Temperature Stress Tests

Once ended the temperature step stress perform the **Extreme Temperature Stress tests**:

1. From ambient temperature decrease temperature at the minimum of the chamber at the maximum pace allowed by the chamber.
2. Let the temperature stabilize for 15 mins
3. Perform the functional tests.
4. Power cycle the board
5. Perform the functional tests.
6. Go to the maximum temperature allowed by the chamber at the maximum pace.
7. Let the temperature stabilize for 15 mins
8. Perform the functional tests
9. Power cycle the board
10. Perform the functional tests.

3.2.1 Optional tests

Vibration Stress Tests

The most effective vibration system for HALT is a Repetitive Shock (RS) with a wide frequency and acceleration range and 6 degree-of-freedom vibration.

An RS shaker, designed to provide energy from 2 Hz to 10000 Hz will do this most effectively.

1. Vibration stress starts at a level of 4 Grms for 10 minutes
2. Power cycle
3. Functional test
4. Increase in the vibration level in 4 Grms for another 10 minutes
5. Power cycle
6. Functional tests
7. Loop until the limit of the chamber or catastrophic failures appear.

Vibration plus Extremes Thermal Rates of Change Tests

This test combines thermal and vibration.

The temperature is ramped as it was during the “*Extreme Temperature Stress*” tests while, at the same time, the vibration is also increased as defined in the “*Vibration Stress*” tests

3.2.3 Some Considerations

The number of products/boards could be lower than the proposed set (4 to 6) when fewer products/boards are available. This by no means signifies that the standard procedure should be escaped. The test will be applied to the complete set as soon as they are available.

Some of the tests can be applied alone in order to accelerate the improvement of the boards. In any case the complete set of HALT tests must be applied.

Regarding relative humidity it will be set in the range of 35 -70 %.

3.3 HALT DOCUMENTATION

For each HALT test a report should be generated. Each report should contain the following:

1. Description of product and its stage of development
2. Specific goals for testing including target stress goals if defined
3. Serial number for product under tests
4. Test equipment list including serial numbers and software revision levels
5. Functional tests description and procedure
6. Test conclusions

4 HASS

4.1 Requirements

The HASS test will be applied to **all devices** of the types selected to pass the HASS tests, in principle all the electronics boards, at least in the early life of the product. As long as the production is advanced and the reliability is correctly assessed the HASS tests can be applied only to a partial number of products or to only some batches.

The following list shows which products should pass the HASS tests:

- Electronics (all the products described in point 3.1)
- DOM
- DU-BASE containers
- JB
- BoB
- VEOC
- Penetrator
- Laser Beacon (including the electronics)
- LBL (including the electronics)

4.2 Description and procedure of the HASS test

4.2.1 Temperature (and vibration)

The procedure to apply to the HASS tests uses temperature (minimum tests). The use of vibration at the same time is also open as an option. The temperature is ramped between its limits (with short pauses at the ends) and vibration, if applied, is maintained at a constant level. A chamber with a thermal cycling with transition rate greater than 10°C/min is recommended. In case of use vibration, a chamber is needed with 6 degree-of-freedom random vibration.

The product, in the case it is a board, should be powered on and with load. Power cycling stress should also be used.

Note:

In order to avoid failure due to dew point (around 5 to 10°C) a first cycle should be performed with boards not powered on in order to identify the condensation level and the associated risk.

2 solutions:

-Fill the facility with nitrogen

-Or power off during cycling the electronic when the temperature is closed to the dew point

- **Temperature (minimum test):** limits at 80% of the UDL and LDL determined from HALT
- **Vibration (optional):** the initial maximum vibration level of HASS/HASA should be at 50% of the vibration destructive limit (DL) but not exceed its operation limit (OL) found during HALT. It will begin at 3 Grms and slowly ramped to the maximum level (50 % of the HALT DL). Vibration will be applied in one five minutes period prior to thermal cycling and for five minutes in a 15 minutes after the defect free thermal cycling

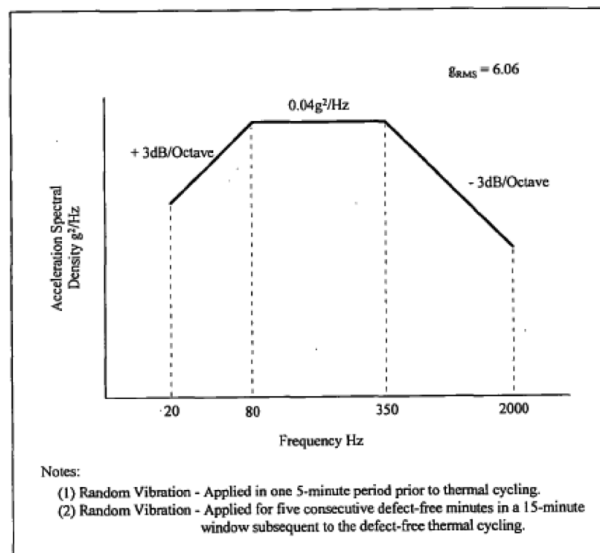


Figure 2: Vibration stress test

- **Testing definition:** The minimum dwell time should be no less than 5 minutes. The dwell time began after the product reached its desired stable temperature. The minimum requirement for vibration is at least 5 minutes at the maximum vibration level plus slow ramped vibration modulation.
- **Cycles Times (based on MIL-HDBK-2164):** the thermal cycling (plus vibration) should be running for 12 cycles as during at least 40 hours for the pre-defect free period. The goal of this period is to remove youth failures. The cycle time shall be adjusted based on the actual products and the test effectiveness. The cycling duration recommended is 3 hours 20 minutes with ramp up and ramp down of $10^{\circ}C$ per minute. An additional defect free period will be performed in order to check that only random failure occurs (youth failure should be removed during the first period). Then the failure rate should conform to the random failure rate awaited for the equipment. In other words, in the defect free period the equipment must operate without failure. By using a feedback loop procedure we can determine if the screening program should be modified. The maximum screening duration should be 120 hours including 40 hours defect free period. Power ON/OFF cycles will be performed in order to electrically stress the equipment as shown in figure 3 (see IPC9592). Dry air will be used in order to control the humidity inside the climatic chamber (avoid moisture development and shorts due to humidity).

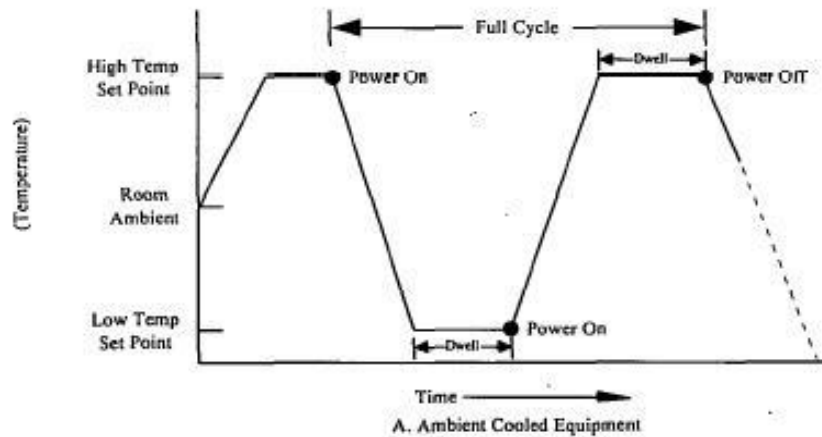


Figure 3: cycling example

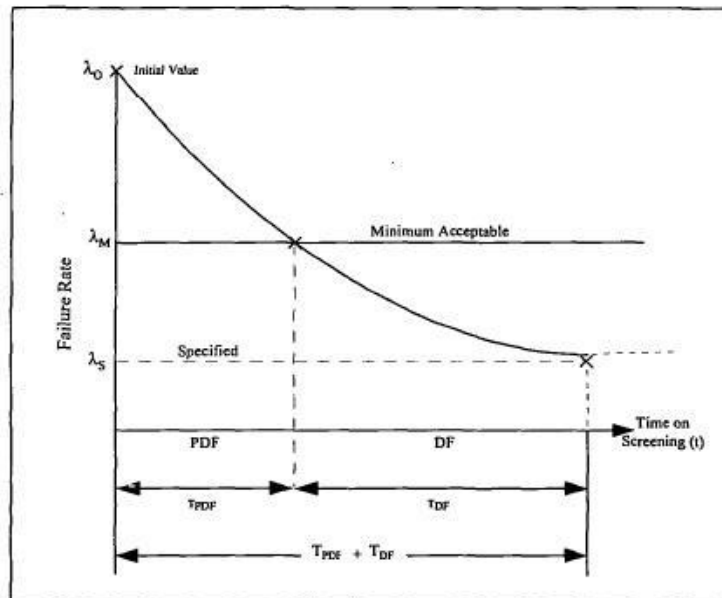


Figure A-1 ESS Characteristics Curve

Figure 4: All youth failures must be removed during the pre-defect period (DF)

- **Proof-of-Screen:** To determine the final cycling profile a proof-of-screen must be performed before the HASS test is applied. It will consist in repeating at least 10 times the initial proposed profile to a subset of boards. If not failures are detected after the first super cycle, (where it is considered that infant mortal is removed). Then, the profile can be considered safe (or not too strong), and can be considered ready to be implemented in the HASS tests to apply to the manufactured boards. If failures are detected, then, the HASS cycle should be reconsidered reducing the level of stress (limits of temperature and/or vibration obtained from HALT) applied and the **proof-of-screen** repeated with the redefined cycling profile.
- **Burn-in:** The HASS tests will include a burn-in phase with a duration from 3 to 24 hours as shown in Figure 5: Burn in + ESS test principle. For the burn-in phase, the IPC9592

standard, appendix F recommends an ambient temperature chamber of 50 to 55°C that mean 65 to 70°C on the powered board with component dissipation.

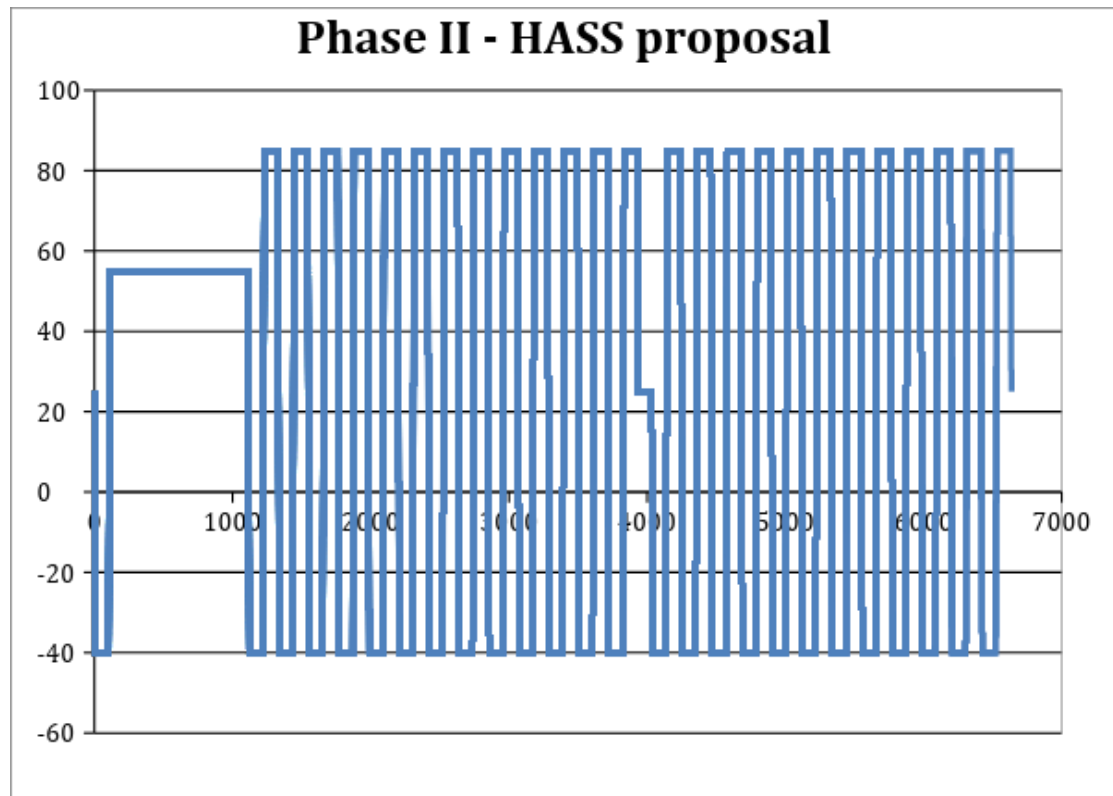


Figure 5: Burn in + ESS test principle for proof

In the Figure 5 above:

- LOL is for the example set at -40°C
- UOL is for the example set at 85°C
- Ambient temperature is set at 25°C
- Burn-in temperature is set at 55°C
- Power ON and OFF cycle are performed at each cycle as shown in Figure 3